# Mahlet Multiport Steer

## Product Brief

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Solutions for Networks

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# 1. Introduction

The Mahlet Multiport Steer (MPS) is an FPGA core that will forward incoming 10G Ethernet frames to 1 of n output ports based on the hash of the IP header or the value of the IP header protocol field. Non-IP frames can be routed to an output port based on user-input.

The MPS core can configured to have up to 4 input ports and 16 output ports. Each input port can handle a full line rate 10G Ethernet stream. Output ports that are oversubscribed can have frames routed to a user-designated overflow port or have the frame dropped.

Forwarding can be based on a list of specific hash or protocol values or a range of hash or protocol values.

# 2. Key Features

- Core is build-time configurable to number of input and output ports
- Operates at full 10G line rate with 64-byte frames
- Frames are stored in internal Block RAM
- Streaming input/output busses use the Avalon Streaming Interface
- Processor Interface port uses Avalon Memory-Mapped Interface
- MPS forwarding tables can be updated while processing traffic
- Non-IPv4 traffic is routed to a user-defined port
- Software-accessible frame counts are available at key points in the core
- Internal storage can be sized using generics
- Can operate stand-alone or in conjunction with the Mahlet IP Filter

# 3. MPS Block Diagram

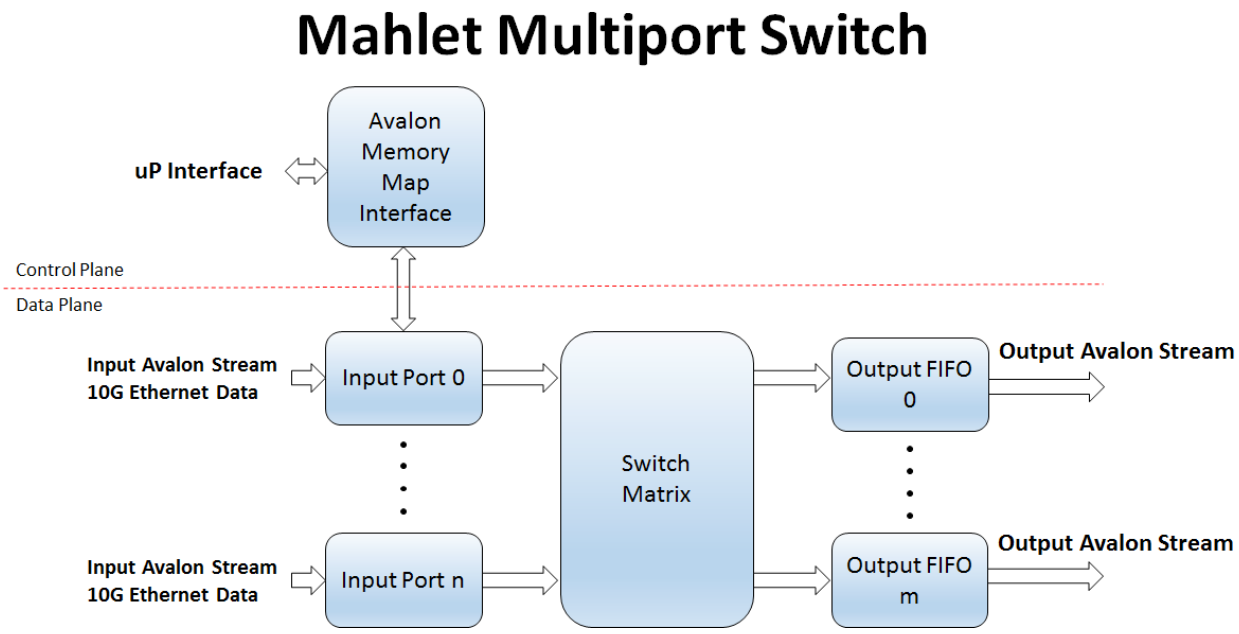


*Figure 1: Mahlet MPS Block Diagram*

# 4. MPS Operations Overview

4.1. FPGA Core Generic Configuration

- Set number of input ports (1 – 4)
- Set number of output ports (1 – 16)
- Select Mahlet IP Filter input mode
- Set FIFO size

4.2. Software Configuration

- Control software selects hash or protocol mode
- Control software selects range or list mode
- Forwarding table update can take place without process interruption
- Forwarding table entries can be deleted at any time using control software
- Software can read frame counts at several points in MPS
    - Each input port
    - Each output port
    - Overflow frames
    - Dropped frames

4.3. Traffic Processing

- Software controls internal forwarding table

- If receiving 10G frame from IPF, a prepended header is read to determine hash or protocol. Else, hash or protocol is extracted from IP header
- Hash or protocol is checked against forwarding table
- If match is found in forwarding table, frame is switched to corresponding output port. Else, frame is dropped
- Non-IP frames are forwarded to a user-defined port
- Frames forwarded to a full port are switched to the overflow port

# 5. MPS Implementation Summary

The following is a summary logic and memory utilization of the MPS when configured for 4 inputs and 8 outputs

| **Vendor** | **Device** | **Logic (ALMs)** | **Memory (bits)** | **Freq (MHz)** |
|---|---|---|---|---|
| Altera | Stratix V GX | 5757 | 10845184 | 156.25 |

# 6. References

Avalon Interface Specifications:

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/manual/mnl_avalon_spec.pdf

# 7. Contact Info

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# 8. Revision History

| Date | Revision | Change |
|---|---|---|
| 1-5-2016 | 0.1 | Initial Document |
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