Mahlet IP Filter

Product Brief

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Solutions for Networks

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1. Introduction

The Mahlet IP Filter (IPF) is an FPGA core that will filter an incoming 10G Ethernet stream based on a user-defined, run-time accessible 4 or 5 Tuple filter table. Incoming frames that match one or more of the filter table entries will be routed to a “pass” output port and non-matching frames will be routed to a “drop” output port.

The five tuples are defined as Source IP Address, Destination IP Address, Protocol, Source Port and Destination Port of the IP header. Four tuple operation omits the Protocol.

The user can specify a filter entry using all members or a subset (wildcard match) of the Tuple set.

2. Key Features

- Core is build-time configurable for 4 or 5 Tuple operation using generics
- Operates at full 10G line rate with 64-byte frames
- Filter table stored in internal Block RAM
- Streaming input/output busses use the Avalon Streaming Interface
- Processor Interface port uses Avalon Memory-Mapped Interface
- Filter table can store up to 500K entries
- Filter table can be updated while processing traffic
- Non-IPv4 traffic is routed to the “drop” port
- Incoming IP stream can be encapsulated with up to two VLAN headers
- Software-accessible frame counts are available at key points in module
- Wildcard filter entries
- IPF FIFOs can be sized using generics
- Can be configured to interoperate with the Mahlet Multiport Steering Engine

3. IPF Block Diagram

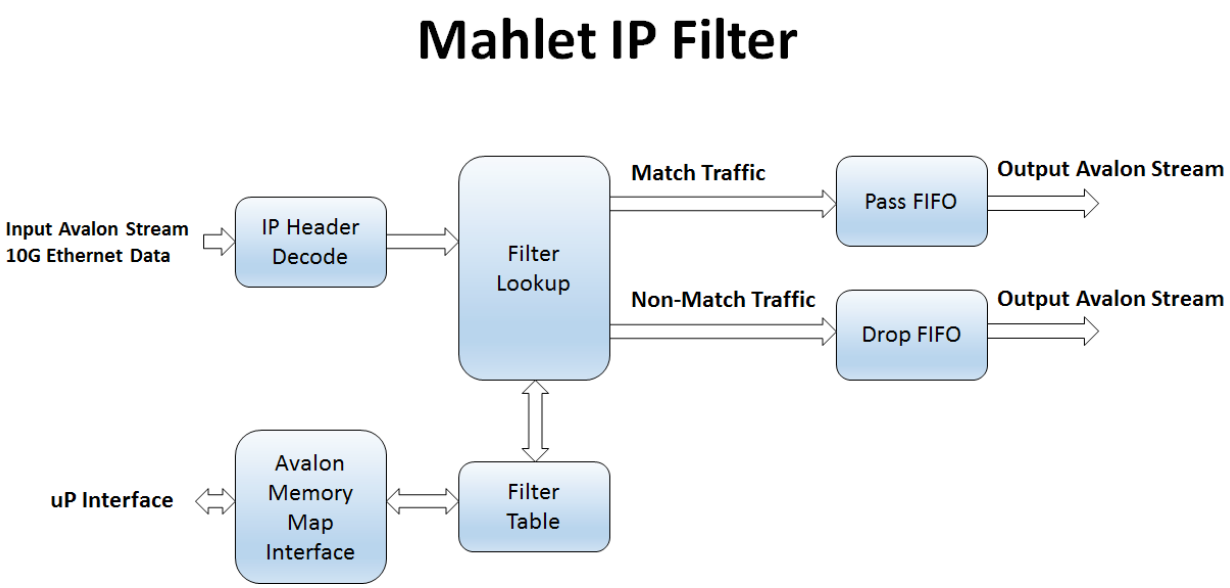

Figure 1: Mahlet IPF Block Diagram

4. IPF Operations Overview

4.1. FPGA Core Generic Configuration

- Select 4 or 5 Tuple Operation
- Select Output Prepend for Mahlet Multiport Steering Engine interface
- Select Optional Test Stream Input

4.2. Software Configuration

- CLI accepts user 4 or 5 Tuple filter entry
- Control software converts user filter entry into proper format for filter table
- Filter table is update with new entry
- Filter table update can take place without process interruption
- Filter table entries can be deleted at any time using software
- Software can read packet counts at several points in IPF
    - IPF Input port
    - Matched Frames
    - Non-Matched Frames
    - Hits per Hash Table Entry

4.3. Traffic Processing

- Software controls internal filter table

- Incoming 10G Ethernet frame is parsed to find start of IP Header
- Source Address, Destination Address, Protocol, Source Port and Destination Port are extracted from IP header
- Hash value is calculated from 4 or 5 tuple input
- Hash value is computed taking CIDR rules into account
- Hash value is used as look-up into filter table
- Filter table returns match or non-match indicator
- Frame is passed to either “pass” or “drop” port
- Non-IP frames are routed to “drop” port

5. IPF Implementation Summary

The following is a summary logic and memory utilization of the IPF configured for 4-tuple operation.

Vendor	Device	Logic (ALMs)	Memory (bits)	Freq (MHz)
Altera	Stratix V GX	2406	7203850	312.50

6. References

Avalon Interface Specifications:

https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/manual/mnl_avalon_spec.pdf

7. Contact Info

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8. Revision History

Date	Revision	Change
1-4-2016	0.1	Initial Document